

Abstract

The invention relates to a method and circuit for synchronizing two signals triggered by clocks of different frequencies, which samples the lower frequency write-enable signal at both positive and negative edges of the higher frequency clock. If the sampling result at the positive or negative edge of the higher frequency clock is “1”, the state is recorded to be a “lock state” and no sampling is taken from the next opposite edge. If the sampling result at the positive or negative edge is “0”, the state is recorded to be a “sampling state” and the next opposite edge will be sampled. Finally, the sampling results taken at the positive and negative edges are joined to output a synchronized write-enable signal.